

Model Name: GA-H61M-D2H-USB3

Revision 1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A 1,2
08	DDR III CHANNEL B 1,2
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*1 SLOT/CLK GEN
16	ITE 8728
17	KB_MS,R_USB,-PROCHOT,RI
18	HWM,FAN CTRL,OV,COMB,LPT
19	DUAL BIOS
20	FP,F_USB,SPKR,SATA LED
21	AUDIO ALC889
22	REAR AUDIO JACK
23	ATHEROS AR8151/USB_LAN
24	HDMI/DVI
25	DISCRETE POWER
26	ATX
27	ISL95870_CPU_VTT

SHEET

TITLE

28	VCORE ISL6364_1
29	VCORE ISL6364_2,VAXG
30	VCORE ISL6364_3,VCORE
31	Etron USB3.0
32	IT8892E
33	PCI SLOT 1.2

Gigabyte Technology			
Cover Sheet			
Title	GA-H61M-D2H-USB3		
Size	Document Number	Rev	1.0
Custom			
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Model Name: GA-H61M-D2H-USB3 *Revision1.0*

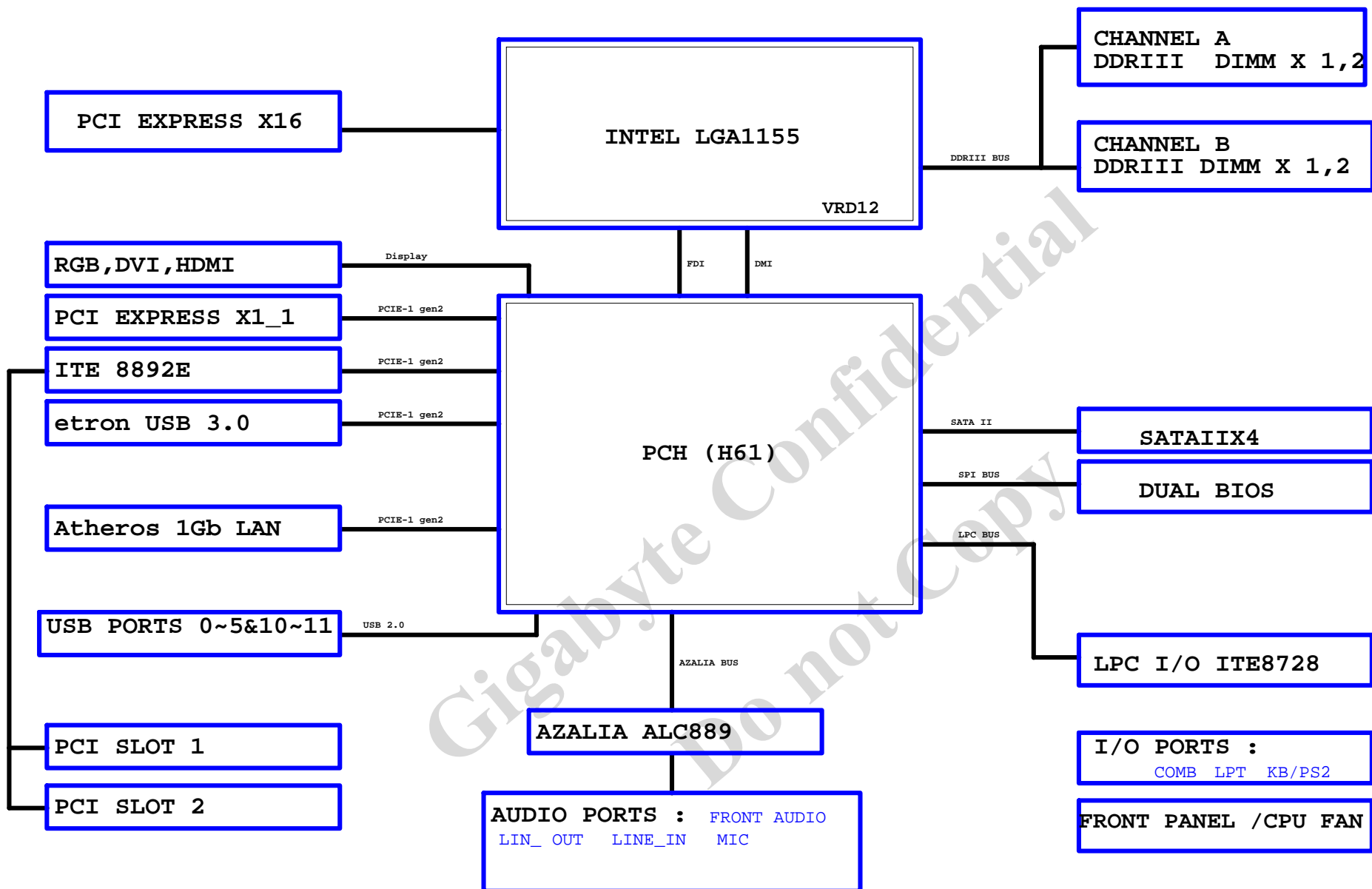
Circuit or PCB layout change

Component value change history

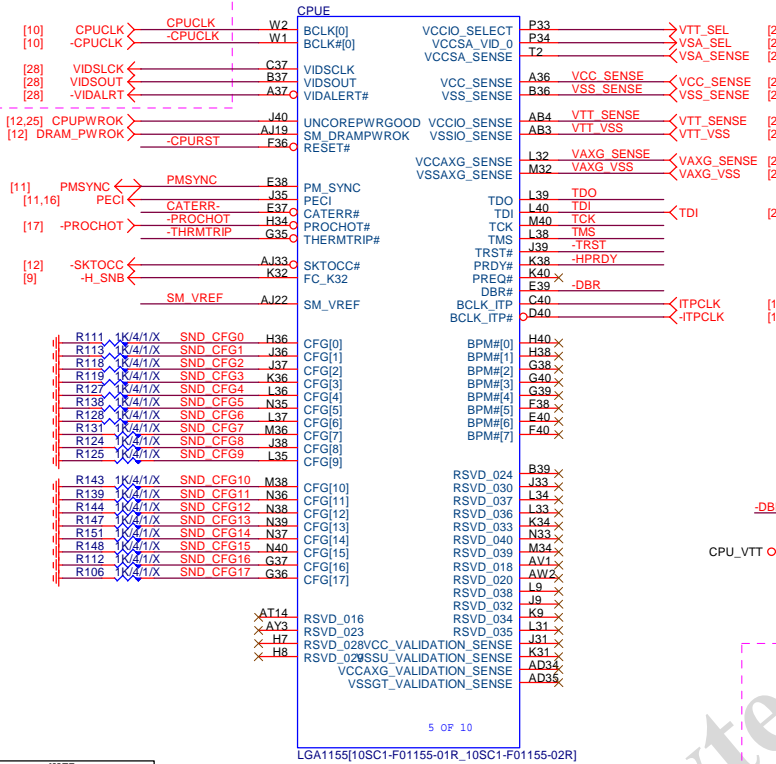
2011/03/25

[illegible][illegible]

BLOCK DIAGRAM



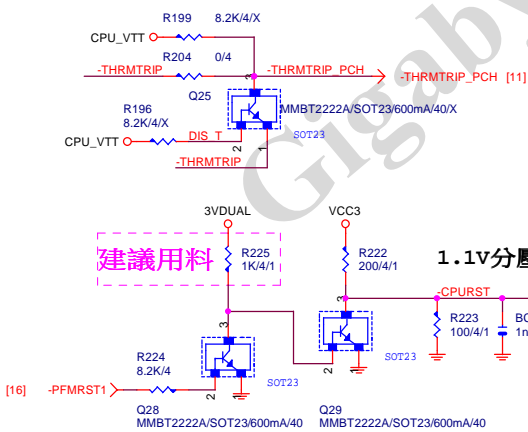
R88 R93 R92 0 change to short



CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	NORM	Reverse	LANE REVERSAL[0],x16
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1x16, Default
1	0	ZX8
0	1	RSVD
0	0	X8,X4,X4

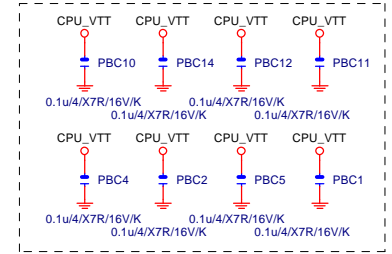
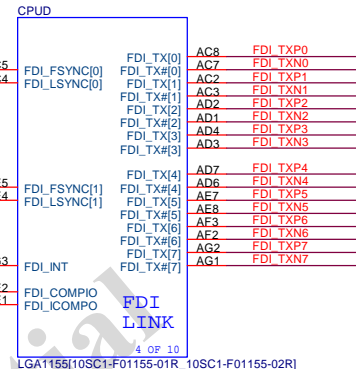
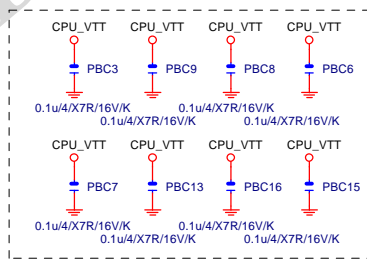
CFG 0-17 all internal PULL-UP



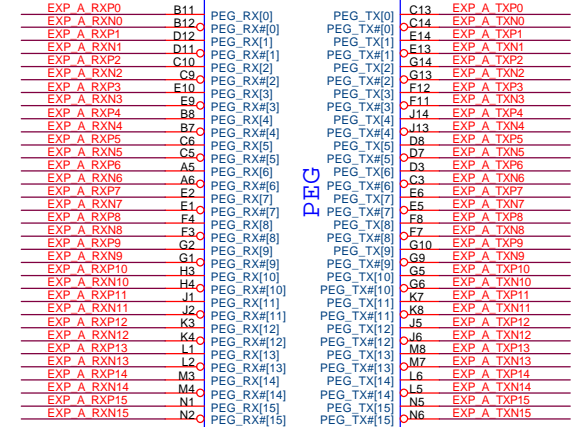
R208 R103 R156 R154 change to RN
R91 75 change to 100
R90 121 change to 100



Stitching caps for PCIE,DMI,FDI bus



Stitching caps for PCIE,DMI,FDI bus



Gigabyte Technology

CPU LGA1155-A		
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CPUA

MAAA0	AV27	SA_MA[0]	SA_DQS[0]	AK3	DQSA0
MAAA1	AY24	SA_MA[1]	SA_DQS[0]	AK2	-DQSA0
MAAA2	AW24	SA_MA[2]			
MAAA3	AW23	SA_MA[3]			
MAAA4	AV23	SA_MA[4]	SA_DQ[0]	AJ3	MDA0
MAAA5	AT24	SA_MA[5]	SA_DQ[1]	AJ4	MDA1
MAAA6	AT23	SA_MA[6]	SA_DQ[2]	AL3	MDA2
MAAA7	AU22	SA_MA[7]	SA_DQ[3]	AL4	MDA3
MAAA8	AV22	SA_MA[8]	SA_DQ[4]	AJ2	MDA4
MAAA9	AT22	SA_MA[9]	SA_DQ[5]	AJ1	MDA5
MAAA10	AV28	SA_MA[10]	SA_DQ[6]	AL2	MDA6
MAAA11	AU21	SA_MA[11]	SA_DQ[7]	AL1	MDA7
MAAA12	AT21	SA_MA[12]			
MAAA13	AW32	SA_MA[13]	SA_DQS[1]	AP3	DQSA1
MAAA14	AU20	SA_MA[14]	SA_DQS[1]	AP2	-DQSA1
MAAA15	AT20	SA_MA[15]			

[7]
[7]
[7]

-SWEA <- SCASA
-SRASA <- SRASA

[7]
[7]
[7]

SBA0 <- SBA0
SBA1 <- SBA1
SBA2 <- SBA2

[7]
[7]

-CSA0 <- CSA0
-CSA1 <- CSA1

[7]
[7]

CKEA0 <- CKEA0
CKEA1 <- CKEA1

MODT_A0
MODT_A1

[7]
[7]
[7]
[7]
[7]
[7]
[7]

DCLKA0 <- DCLKA0
-DCLKA0 <- DCLKA0
DCLKA1 <- DCLKA1
-DCLKA1 <- DCLKA1
DCLKA2 <- DCLKA2
-DCLKA2 <- DCLKA2
DCLKA3 <- DCLKA3
-DCLKA3 <- DCLKA3

[7,8] -DDR3_RST <- AW18

C97
0.1u/4/X7R/16V/K/X

AV13
AV12
AV12
AV14
AV13
AV13
AV13
AV11
AV12
AV12

SM_DRAMRST#

DDR_0

1 OF 10

LGA1155[10SC1-F01155-01R_10SC1-F01155-02R]

CPUB

MAAB0	AK24	SB_MA[0]	SB_DQS[0]	AH7	DQSB0
MAAB1	AM20	SB_MA[1]	SB_DQS[0]	AH6	-DQSB0
MAAB2	AM19	SB_MA[2]			
MAAB3	AK18	SB_MA[3]			
MAAB4	AP19	SB_MA[4]	SB_DQ[0]	AG7	MDB0
MAAB5	AP18	SB_MA[5]	SB_DQ[1]	AG8	MDB1
MAAB6	AM18	SB_MA[6]	SB_DQ[2]	AJ9	MDB2
MAAB7	AL18	SB_MA[7]	SB_DQ[3]	AJ8	MDB3
MAAB8	AN18	SB_MA[8]	SB_DQ[4]	AG5	MDB4
MAAB9	AY17	SB_MA[9]	SB_DQ[5]	AG6	MDB5
MAAB10	AN23	SB_MA[10]	SB_DQ[6]	AJ6	MDB6
MAAB11	AU17	SB_MA[11]	SB_DQ[7]	AJ7	MDB7
MAAB12	AT18	SB_MA[12]			
MAAB13	AR26	SB_MA[13]	SB_DQS[1]	AM8	DQSB1
MAAB14	AY16	SB_MA[14]	SB_DQS[1]	AL8	-DQSB1
MAAB15	AV16	SB_MA[15]			

[8]
[8]
[8]

-SWEB <- SWEB
-SCASB <- SCASB
-SRASB <- SRASB

[8]
[8]
[8]

SBAB0 <- SBAB0
SBAB1 <- SBAB1
SBAB2 <- SBAB2

[8]
[8]

-CSB0 <- CSB0
-CSB1 <- CSB1

[8]
[8]

CKEB0 <- CKEB0
CKEB1 <- CKEB1

MODT_B0
MODT_B1

[8]
[8]

DCLKB0 <- DCLKB0
-DCLKB0 <- DCLKB0
DCLKB1 <- DCLKB1
-DCLKB1 <- DCLKB1
DCLKB2 <- DCLKB2
-DCLKB2 <- DCLKB2
DCLKB3 <- DCLKB3
-DCLKB3 <- DCLKB3

[8]
[8]
[8]
[8]
[8]
[8]
[8]

VREF_DQB
VREF_DOA

[8]
[7]

AN16
AN15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

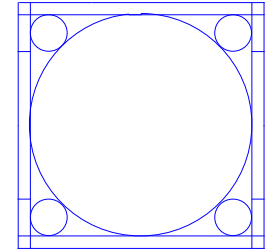
AP16
AP15

[8]
[7]

AL16
AL15

[8]
[7]

AP16
AP15

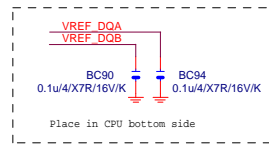
CR
CPU RETENTION/X

Need check the new CPU ME

CPU

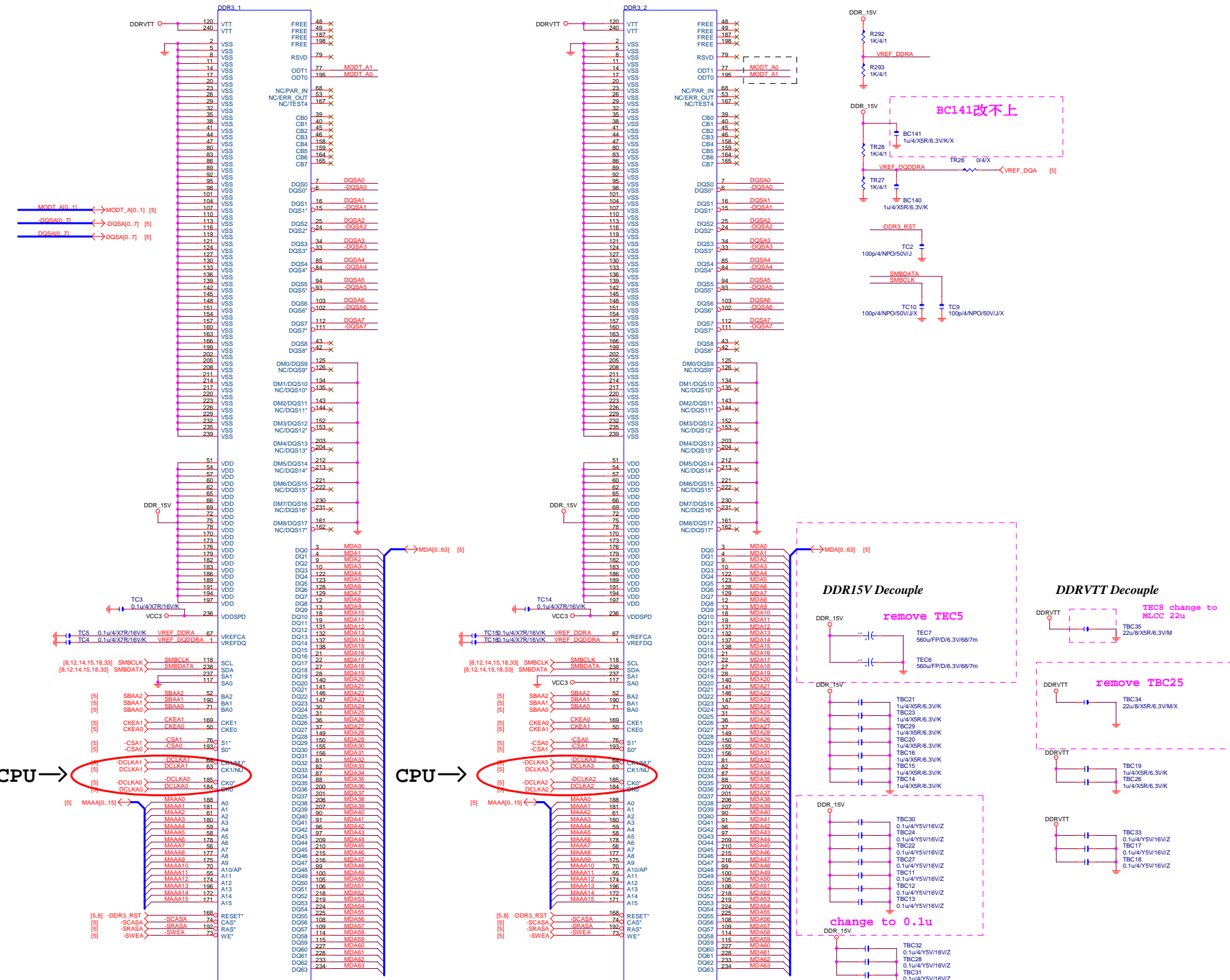


ILM_BP/1156/CSP/[12KRC-0F0001-01R_12KRC-0F0001-04R]

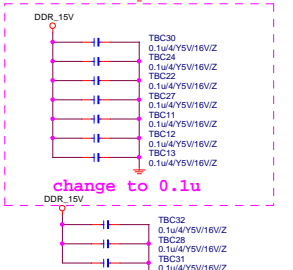
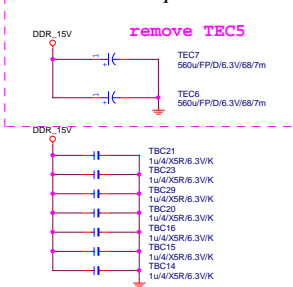


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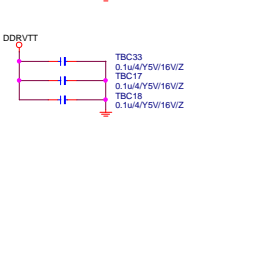
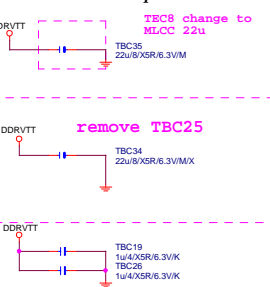
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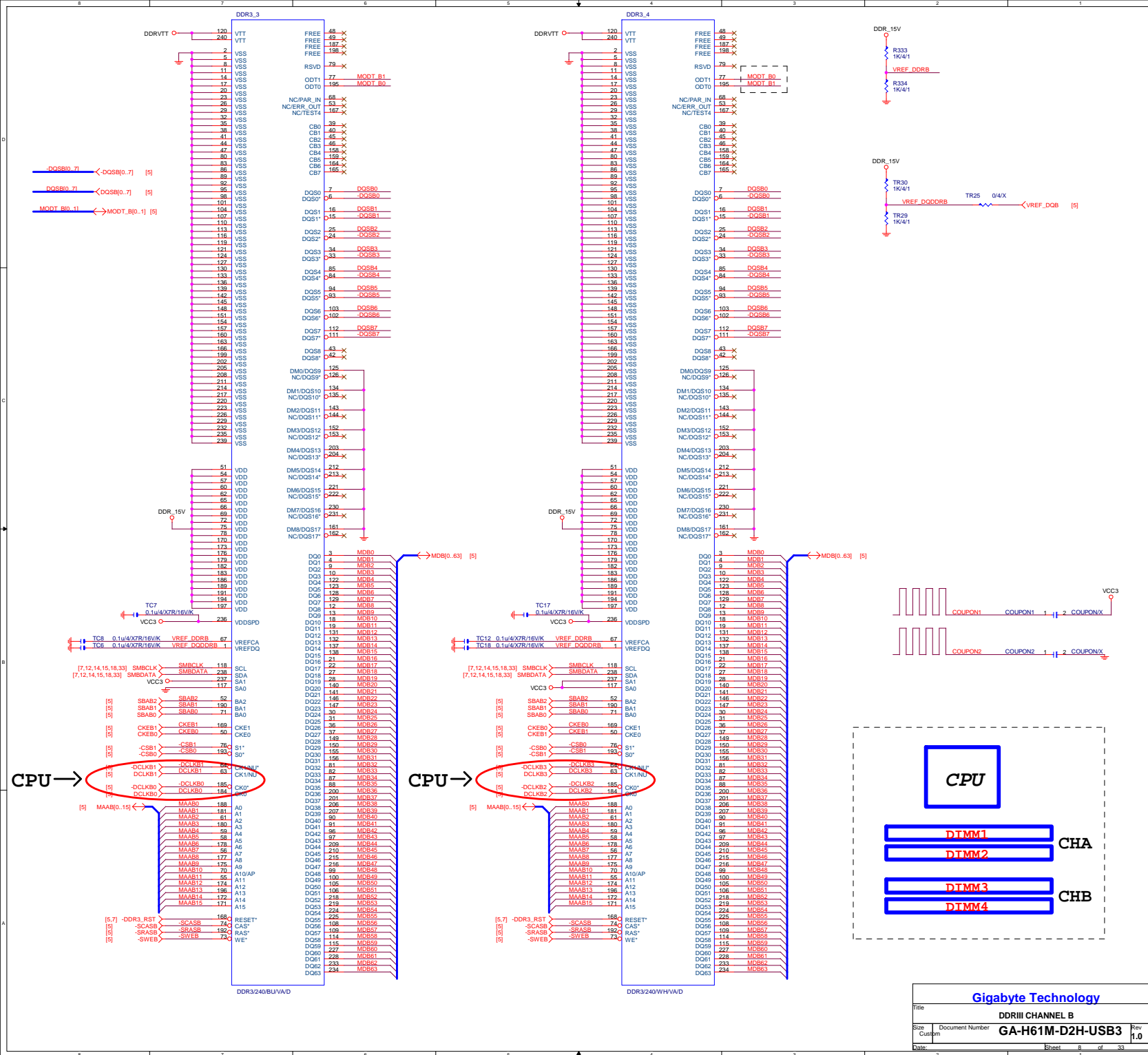
DDR15V Decouple

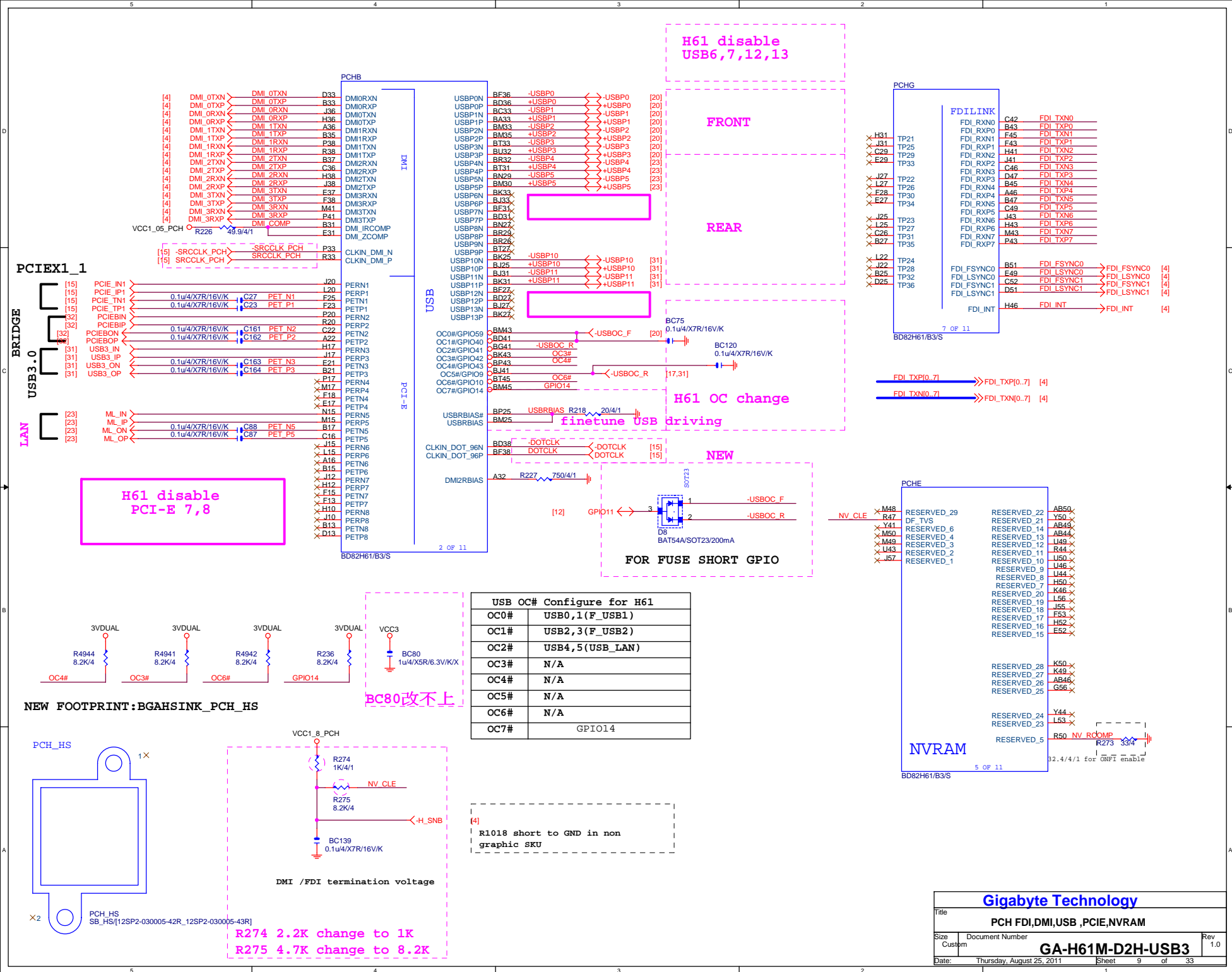


DDRVT Decouple



Gigabyte Technology		
Title	DDR3 CHANNEL A	
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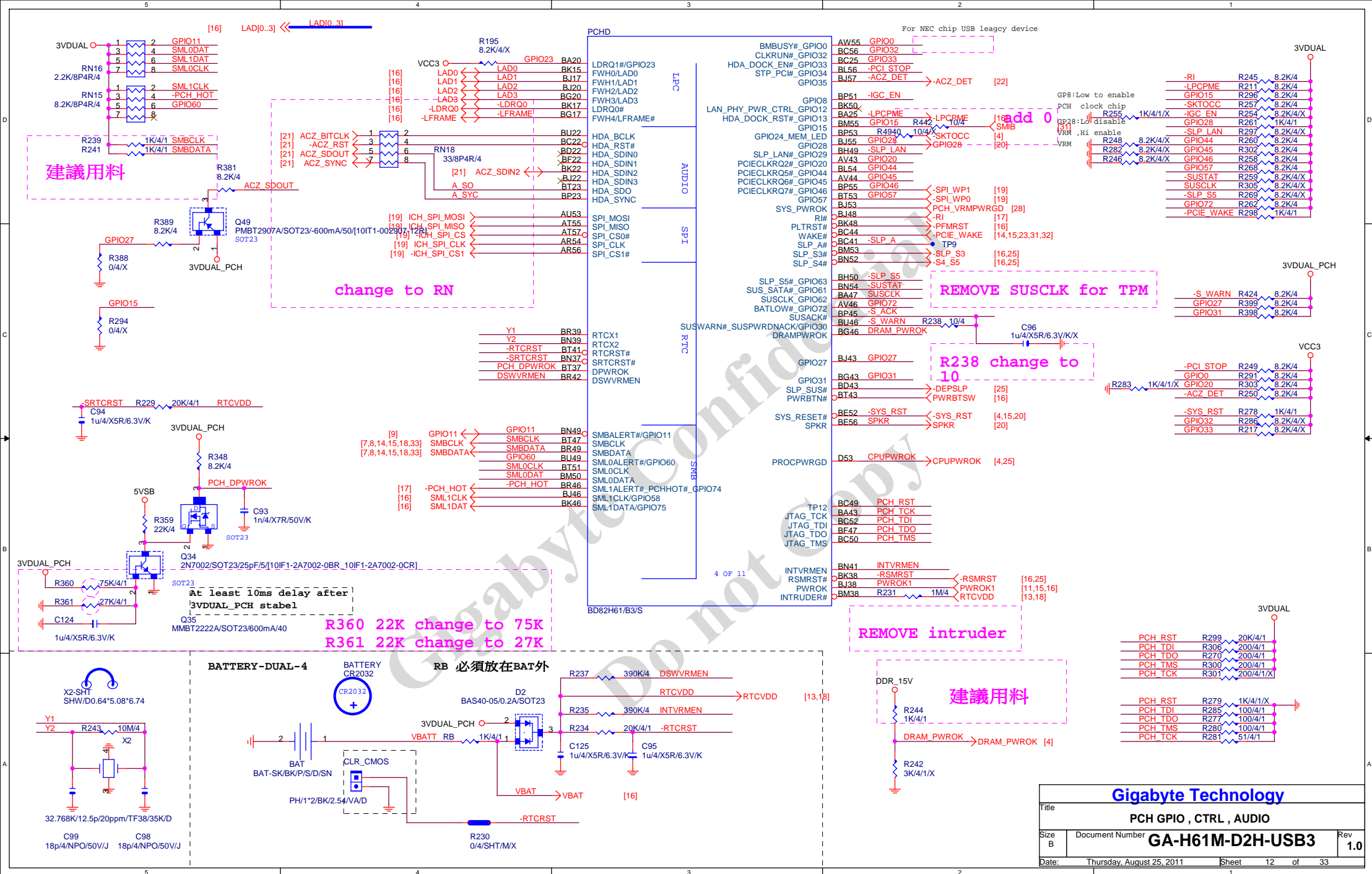


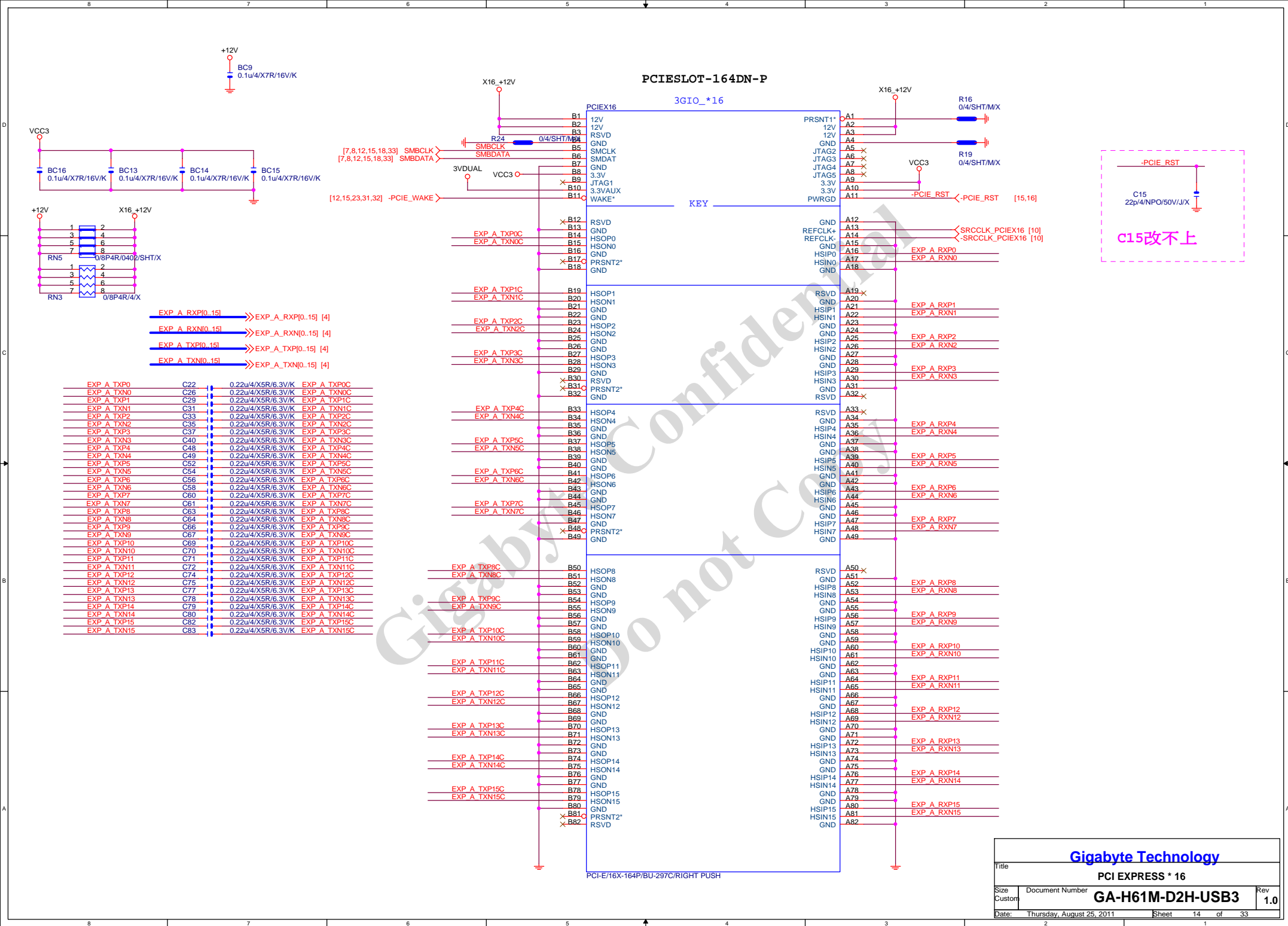


X7-SATA2-HS-MASK

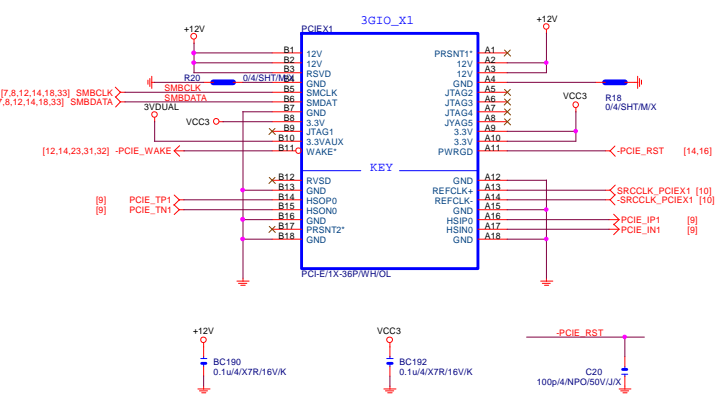


Title			
PCH HOST , SATA, PCI			
Size B	Document Number	GA-H61M-D2H-USB3	Rev 1.0
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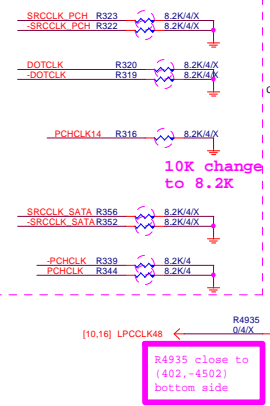




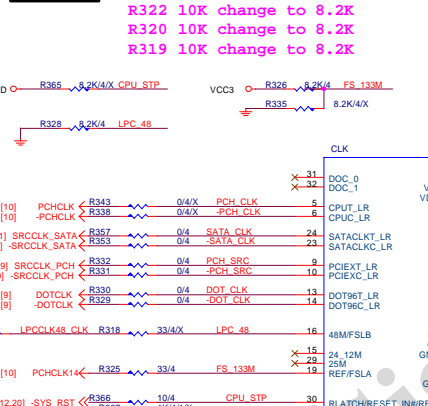
PCIE X1



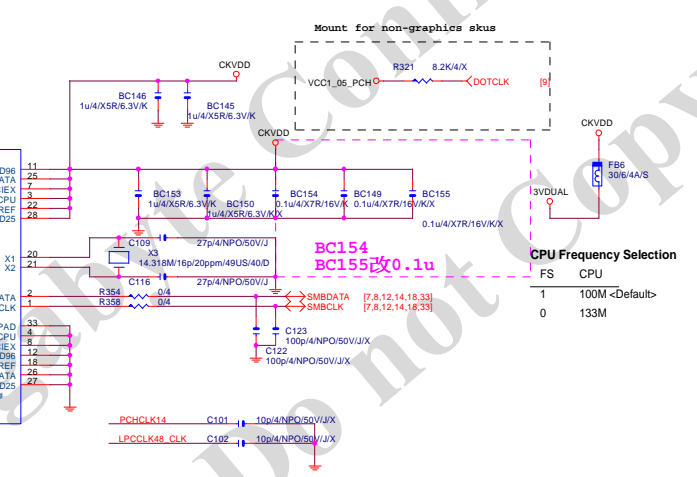
INTERNAL CLK STRAPPING



CLK GEN



建議用料



CPU Frequency Selection

FS	CPU
1	100M <Default>
0	133M

GP22 Default GP22 DIODS

GP23 Default CPU_PG DOD8

REMOVE R146,R149

powerflow change to 3VDUAL_PCH

R109 0 change to 10

FOR AR8161

-PFMRST2 for TPM

REMOVE Q20 R158 & R155 for ITE 8728 DX

IT8728	
PIN121	VCORE_EN#/PCR_C0
PIN120	VLDT_EN#/PCH_D0
PIN19	ATXPG
PIN31	PCR_C1
PIN53	SST/AMDTSI_D#/MTRB#/PCH_D1
PIN55	PECI/AMDTSI_C#/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2 (VCC5)
PIN96	VIN1 (VCC12)
PIN97	VIN1/VDIMM_STR (1.5V)
PIN98	VIN0/VCORE (1.1V)/NC

REMOVE R61 & R141 .R77 R136 改上件 for ITE 8728 DX

R83 R66 change to 10

IT8728F(GB)

ADD LPT PORT

REMOVE ON/OFF CHARGER

建議用料

建議用料

remove IO GP43 pull high

Gigabyte Technology

ITE 8728 LPC IO

GA-H61M-D2H-USB3

Rev 1.0

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REMOVE NR1A- in R1.1

建議用料

[18]

NR1B

D1
BAT54C/SOT23/200mA

R43
75K/4/1

R42
8.2K/4

Q12
MMBT2222A/SOT23/600mA/40

SOT23

-RI → RI [12]

KBDATA

1

6

KBCLK

5

FUSEVCC_R

4

MSCLK

3

ESD18

CM1293A-04SO/S/[10TA1-010009-10R_10TA1-018902-10R]

FUSEVCC_R1

UR2
150K/4

UR3
270K/4

-USBOC_R

-USBOC_R [9,31]

KB/MS

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

2

KB

3

KB/MS/6P/PC99/OS/RA/D/2

AGND1

AGND1

AGND1

MSDATA

7

MSCLK

12

KBDATA

1

KBCLK

The schematic shows four input signals at [16] bits: VREF, SYS_TEMP, DDR_TEMP, and TEMP3. These are connected to a network of resistors and capacitors. R102 (10K/4/1) connects VREF to the first node. R107 (10K/4/1) connects VREF to the second node. R110 (10K/4/1) connects VREF to the third node. C53 (1u/4/X5R/6.3V/K) connects the first node to ground. C55 (1u/4/X5R/6.3V/K) connects the second node to ground. RS2 (10K/1/4/S, Close S10) connects the first node to the second node. C57 (1u/4/X5R/6.3V/K) connects the second node to ground. RS3 (10K/1/4/S, Close DDR) connects the second node to the third node. The output signals are labeled as follows:

- VREF ←
- SYS_TEMP ←
- DDR_TEMP ←
- TEMP3 ←

Component values and labels:

- C53: 1u/4/X5R/6.3V/K
- C55: 1u/4/X5R/6.3V/K
- RS2: 10K/1/4/S, Close S10
- C57: 1u/4/X5R/6.3V/K
- RS3: 10K/1/4/S, Close DDR
- R102: 10K/4/1
- R107: 10K/4/1
- R110: 10K/4/1

REMOVE intruder

[12,13] RTCVDD ← R228 1M/4 → -CASEOPEN → CASEOPEN [16,20]

C65 0.01u/4/X7R/25V/K

Case Open Circuits

The schematic diagram illustrates the power supply circuit for the iZ80, featuring a 2.9V regulator. The circuit is organized into three main sections: CUR_DETECT1, I (VCORE), and CUR_DETECT. The 2.9V regulator is centered around a 2.9V reference and a 10K/4/1 resistor network. The circuit includes various input voltages (VCORE, DDR_15V, VCC3, +12V, VCC) and output voltages (VINO, CPU_VTT). Key components include resistors R95, R98, R232, R69, R58, R68, R59, R70, R85, R46, R86, R67, and capacitors C50, C51, C45, C47, C43. The circuit is divided into sections: CUR_DETECT1, I (VCORE), and CUR_DETECT. The 2.9V regulator is centered around a 2.9V reference and a 10K/4/1 resistor network.

[illegible]

[16] FANPWM3

+12V

R173
0.6/SHT/M/X

+12V

R175
3.3K/4/1

R176
15K/4/1

R182
6.2K/4/1

C81
0.047u/4/X7R/16V/K

FANIO1

CPU_FAN
FAN1*1*4W/A3/PA66

R176
R182建議用料

[16]

Diagram showing the connection of a 12V supply to a fan (SYS_FAN FAN14WHI3/PA66) through a network of resistors (R8, R9, R10, R14) and a capacitor (C11). The circuit includes a 12V supply, a fan, and various components labeled R8, R9, R10, R14, and C11. A callout box suggests R9 and R10 values.

Component values and labels:

- R8: 3.3K/4/1
- R9: 15K/4/1
- R10: 6.2K/4/1
- R14: 0/6/SHT/M/X
- C11: 0.047u/4/X7R/16V/K

Callout box text: R9 R10建議用料

Label: SYS_FAN FAN14WHI3/PA66

Figure 10 illustrates the pin connections for the 33/8P4R/4 module. The diagram is divided into three sections, each showing a different set of pins and their corresponding connections.

PRN1 (Left Section): This section shows connections for pins 1 through 8. The connections are as follows:

- STB (Pin 1) connects to LPT1 (Pin 1).
- STB (Pin 2) connects to LPT4 (Pin 2).
- AFD (Pin 3) connects to LPT16 (Pin 3).
- AFD (Pin 4) connects to LPT17 (Pin 4).
- INIT (Pin 5) connects to LPT16 (Pin 5).
- INIT (Pin 6) connects to LPT17 (Pin 6).
- SLIN (Pin 7) connects to LPT16 (Pin 7).
- SLIN (Pin 8) connects to LPT17 (Pin 8).

PRN2 (Right Section): This section shows connections for pins 1 through 8. The connections are as follows:

- PD3 (Pin 1) connects to LPT5 (Pin 1).
- PD3 (Pin 2) connects to LPT4 (Pin 2).
- PD2 (Pin 3) connects to LPT3 (Pin 3).
- PD2 (Pin 4) connects to LPT2 (Pin 4).
- PD1 (Pin 5) connects to LPT3 (Pin 5).
- PD1 (Pin 6) connects to LPT2 (Pin 6).
- PD0 (Pin 7) connects to LPT3 (Pin 7).
- PD0 (Pin 8) connects to LPT2 (Pin 8).

33/8P4R/4 (Bottom Section): This section shows connections for pins 1 through 8. The connections are as follows:

- ERR (Pin 1) connects to LPT6 (Pin 1).
- ACK (Pin 2) connects to LPT7 (Pin 2).
- BUSY (Pin 3) connects to LPT8 (Pin 3).
- PE (Pin 4) connects to LPT9 (Pin 4).
- SLCT (Pin 5) connects to LPT6 (Pin 5).
- SLCT (Pin 6) connects to LPT7 (Pin 6).
- PD[0..7] (Pin 7) connects to LPT8 (Pin 7).
- PD[0..7] (Pin 8) connects to LPT9 (Pin 8).

[illegible]

R402 change to SHORT PAD

接pwm
feedback
pin

接pwm
feedback
pin

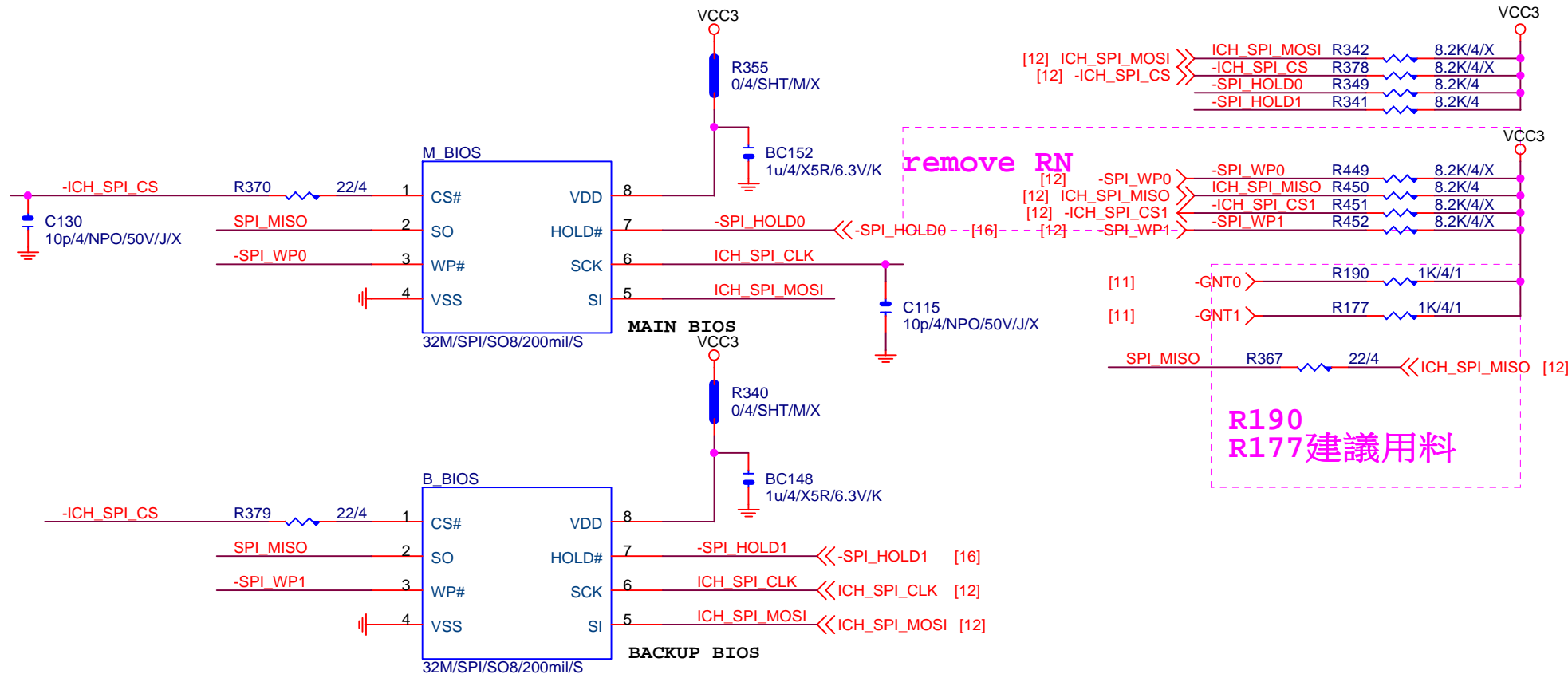
COMB改pinheader
COMB改COMA 1.1

Gigabyte Technology

Title			
HWM,FAN CTRL,OV,COMB,LPT			
Size	Document Number	GA-H61M-D2H-USB3	Rev
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DUAL BIOS

R349 R341 改上件 for ITE 8728 DX



BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

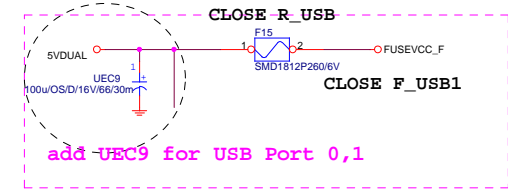
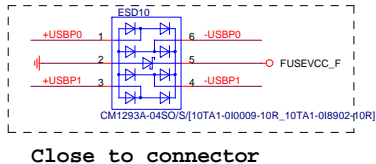
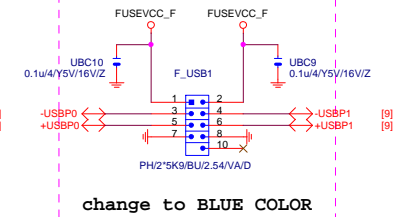
1 means floating
0 means PD 1K

Gigabyte Technology

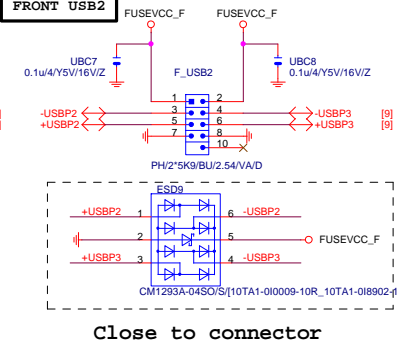
Title		
DUAL BIOS		
Size A	Document Number GA-H61M-D2H-USB3	Rev 1.0
Date:	Thursday, August 25, 2011	Sheet 19 of 33

FRONT USB1

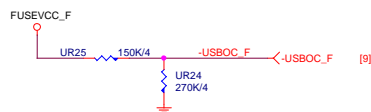
FU改pinheader



FRONT USB2



FU改pinheader

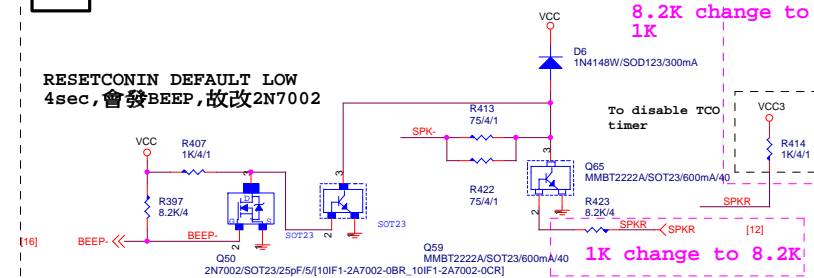


SATA LED



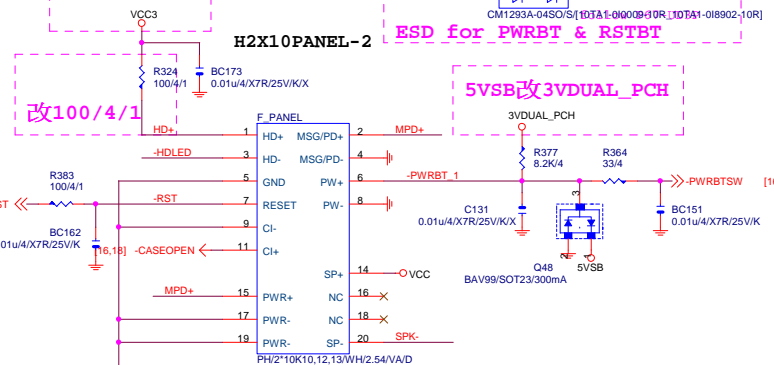
SPKR

RESETCONIN DEFAULT LOW
4sec, 會發BEEP, 故改2N7002

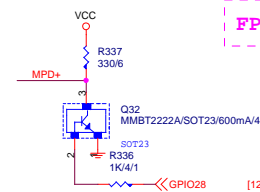


INTEL FRONT PANEL

改VCC3




FP改pinheader

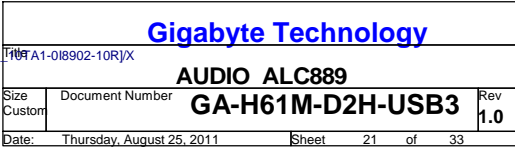


Gigabyte Technology			
Title	FP, F, USB, SPKR, SATA LED		
Size	Document Number	GA-H61M-D2H-USB3	
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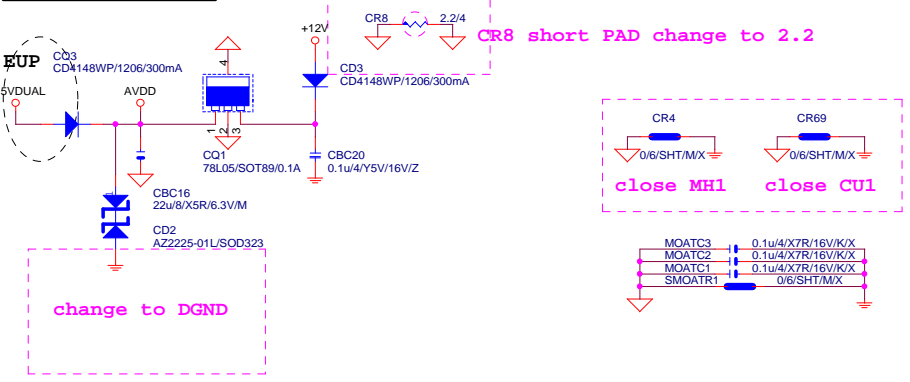
CR28: 20K/4/0.1% @ALC889A
CR28: 20K/4/1% @others



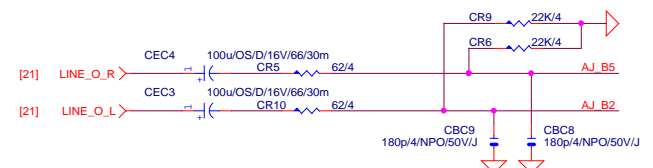
A circuit diagram showing a resistor labeled "20K/4/1" connected to ground. The resistor is represented by a zigzag line. A red line connects one end of the resistor to a common ground symbol, which is a triangle pointing downwards. Another red line extends from the other end of the resistor.



CODEC POWER/EMI PAD

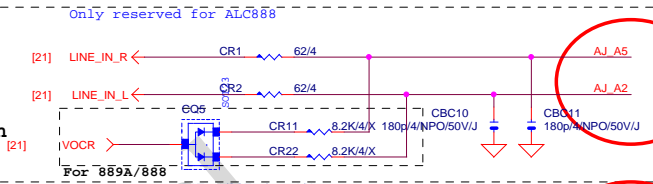


LINE-OUT

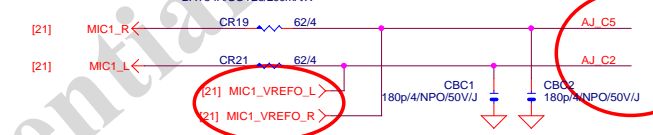


LINE-IN

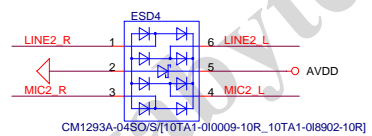
Verify MIC function in LINE-in



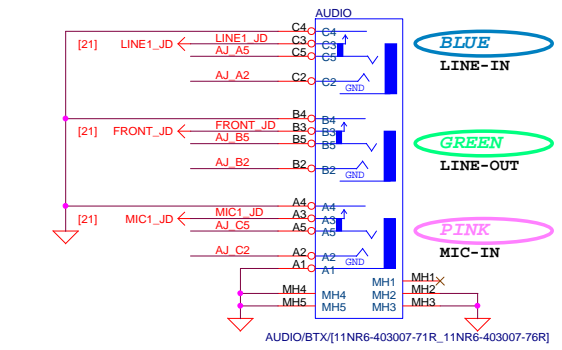
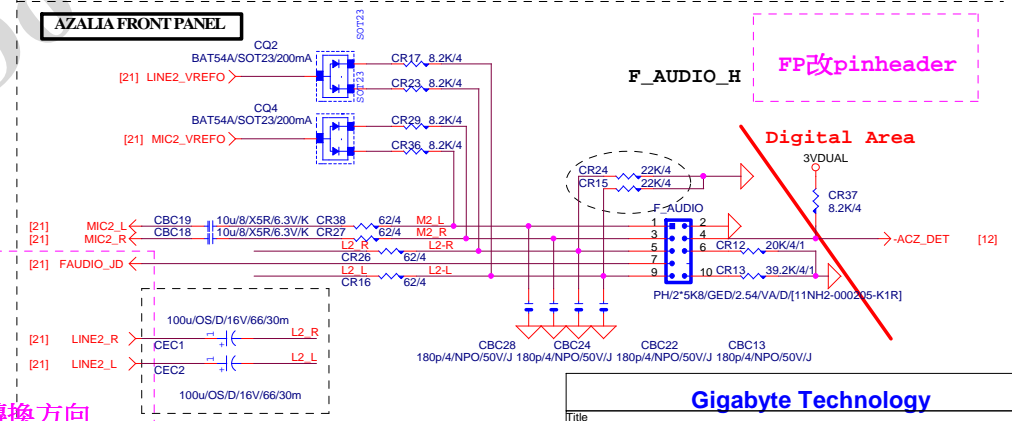
MIC-IN



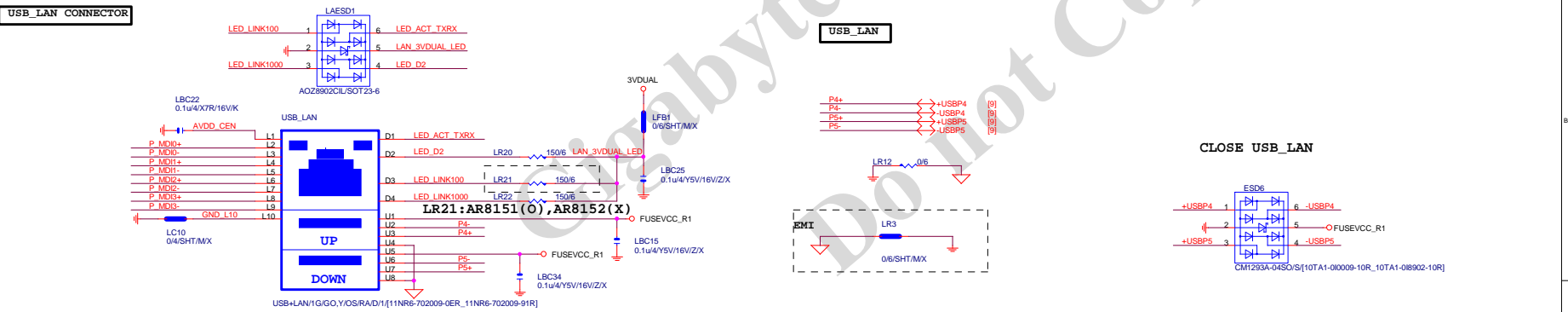
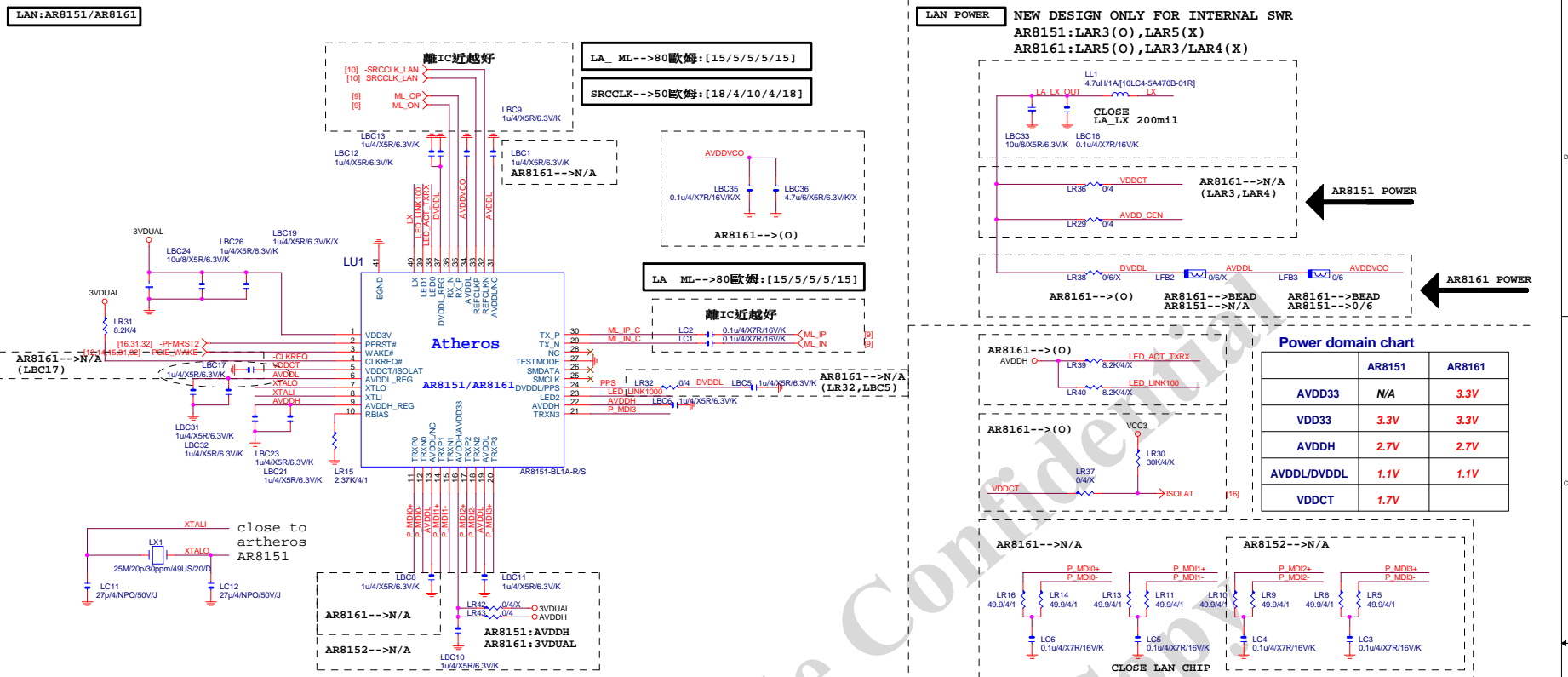
AZALIA JACK



AZALIA FRONT PANEL



Gigabyte Technology			
Title AUDIO JACK			
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料號 規格 廠商

11NR6-702009-0ER	1G LAN (12core)	UDE
11NR6-702009-91R	1G LAN (8 core)	FOXCONN
11NR6-702009-92R	1G LAN (8 core)	UDE
11NR6-702009-11R	1G LAN (12core/RED)	UDE
11NR6-702009-12R	1G LAN (8 core/RED)	FOXCONN

USB LAN BOM區分:

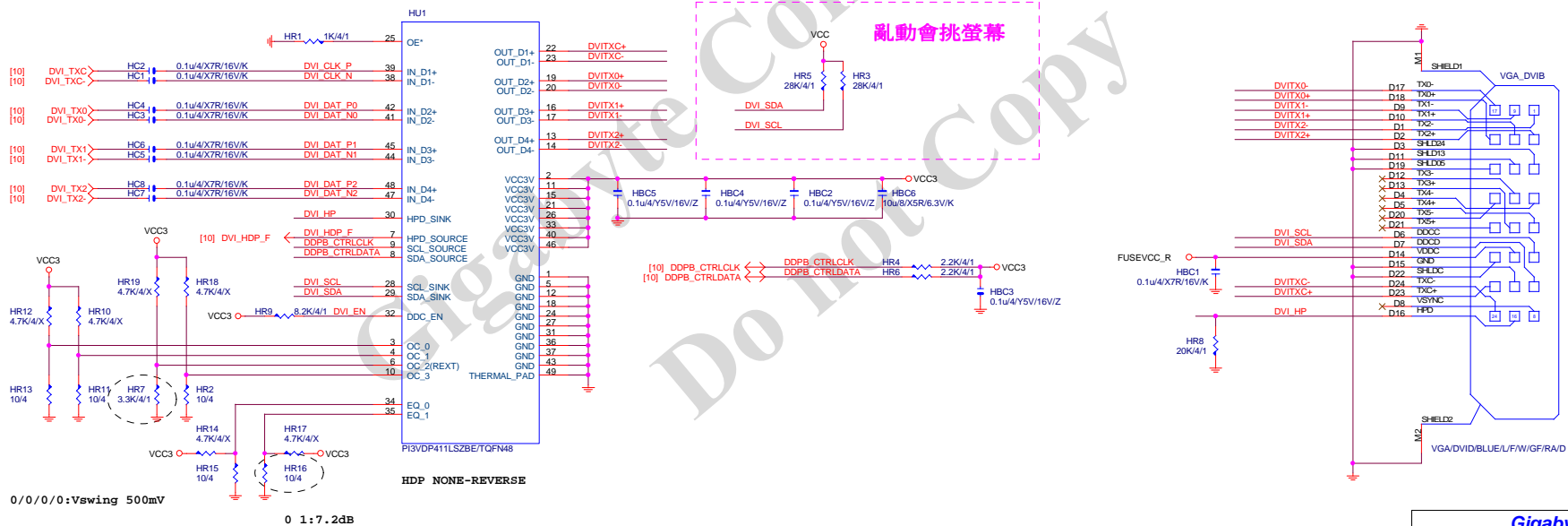
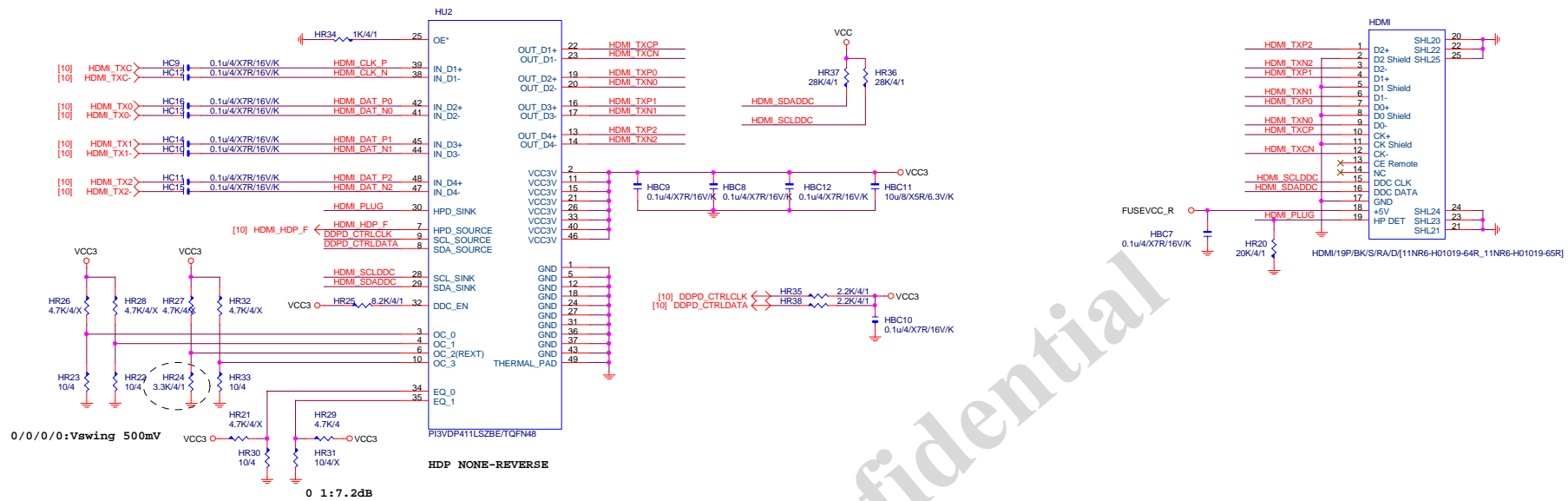
- (紅色/12CORE/三倍): USB+LAN/1G/GO,Y/OS/RA/D/1/RED
- (黑色/12CORE): USB+LAN/1G/GO,Y/OS/RA/D/1
- (黑色/8CORE): USB+LAN/1G/GO,Y/OS/RA/D/8C

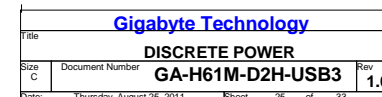
Gigabyte Technology

File ARTHROS AR8151/AR8161

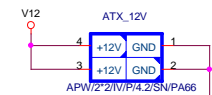
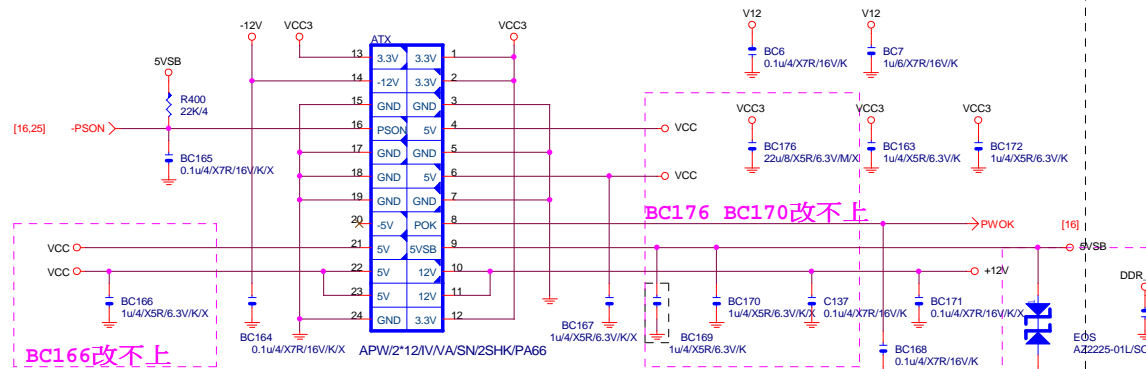
Size Custom Document Number GA-H61M-D2H-USB3

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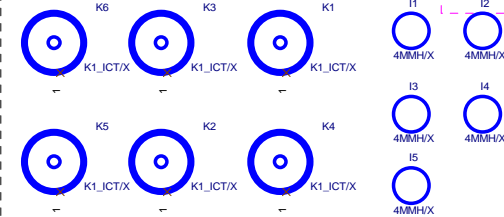
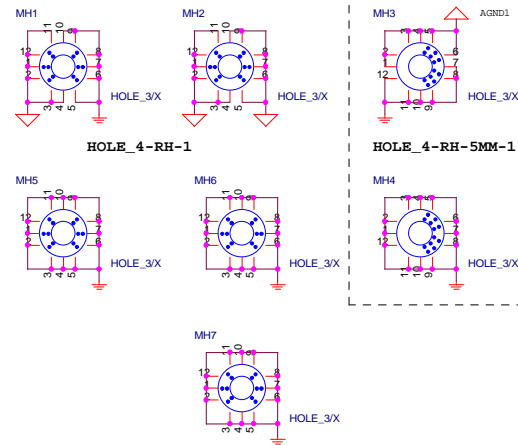




ATXX24 POWER CONNECTOR



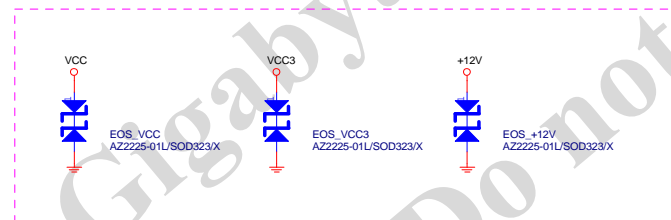
ATX_4-4



```
| To prevent the 5VSB  
| under loading when  
| boot
```

5VDUAL1(USB PORT/DDRIII POWER)
5VDUAL(3VDUAL/OTHER)

```
-S_WARN-->5VDUAL1-->-S_ACK(PCH)-->-DEPSLP/-RSMRST-->5VDUAL-->3VDUAL
```



Gigabyte Technology

ATX CONNECTOR

GA-H61M-D2H-USB3

Rev	1.0
-----	-----

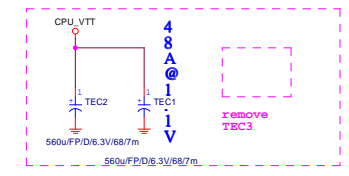
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CPU_VTT

TR23 2K change to 3.83K
 TR23 0 change to 4.02K
 TR22 change to short pad

TR8 0 change to 1
 TR2 0 change to 1
 TR7 0 change to 1

改PPAK & Ferrite Core



	VTT_SEL
HI	1.05V
LO	1.0V

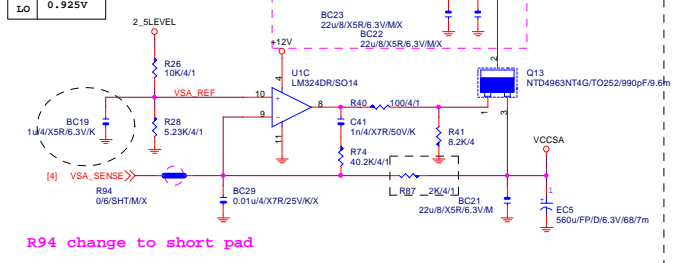
	F_SEL
PU	1MHz
PD	600KHz
NC	500KHz
Sheet GND	300KHz

BOTTOM PAD
 CONNECT TO GND
 THROUGH 4 VIA

VCCSA

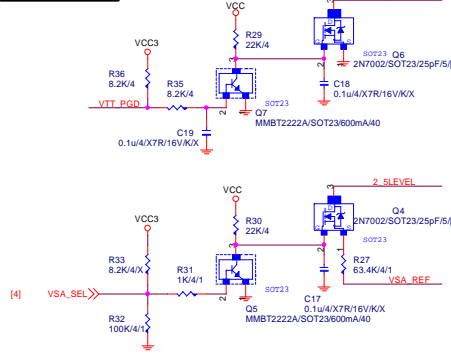
	VSA_SEL
HI	0.85V
LO	0.925V

BC22
 BC23改不上

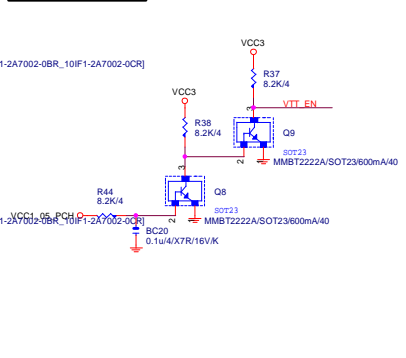


R94 change to short pad

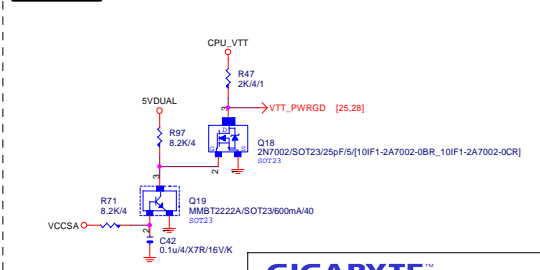
VCCSA PWR SEQ



CPU_VTT PWR SEQ



VTT_PWRGD



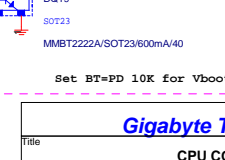
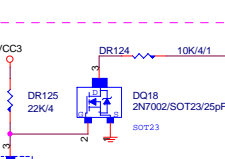
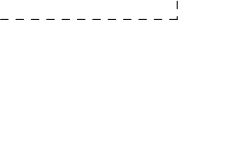
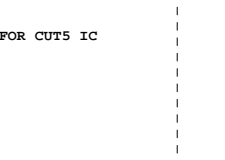
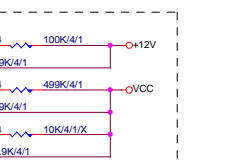
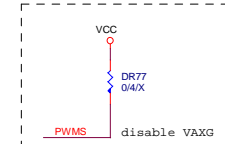
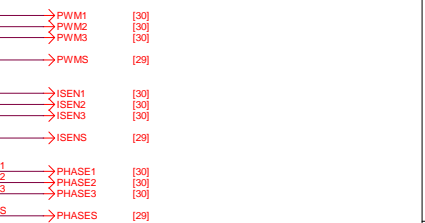
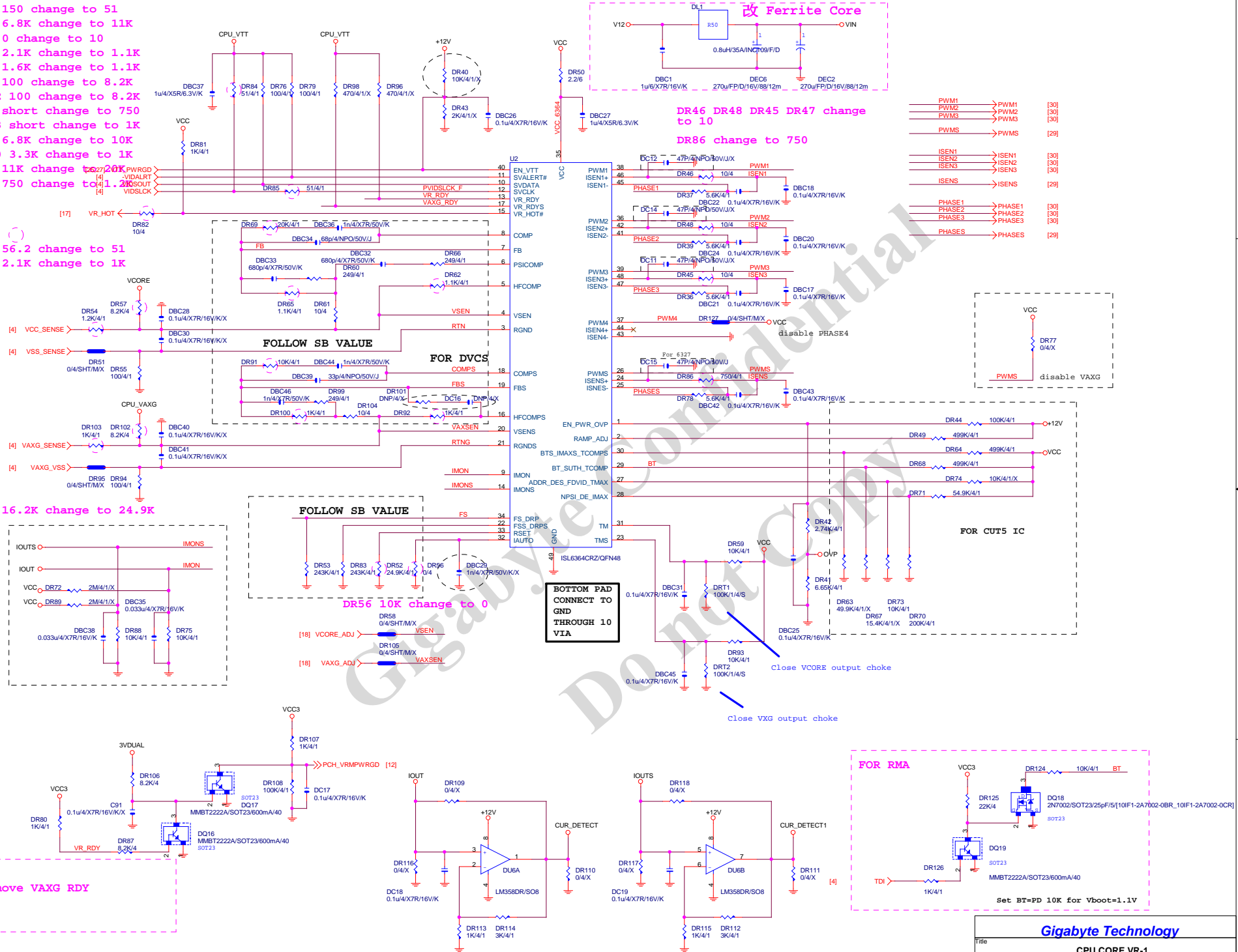
GIGABYTE™			
Title			
CPU_VTT PWM_ISL95870CRZ			
Size	Document Number	GA-H61M-D2H-USB3	Rev 1.0
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DR85 150 change to 51
 DR69 6.8K change to 11K
 DR82 0 change to 10
 DR62 2.1K change to 1.1K
 DR65 1.6K change to 1.1K
 DR57 100 change to 8.2K
 DR102 100 change to 8.2K
 DR54 short change to 750
 DR103 short change to 1K
 DR91 6.8K change to 10K
 DR100 3.3K change to 1K
 DR69 11K change to 20K
 DR54 750 change to 1.2K

DR84 56.2 change to 51
 DR92 2.1K change to 1K

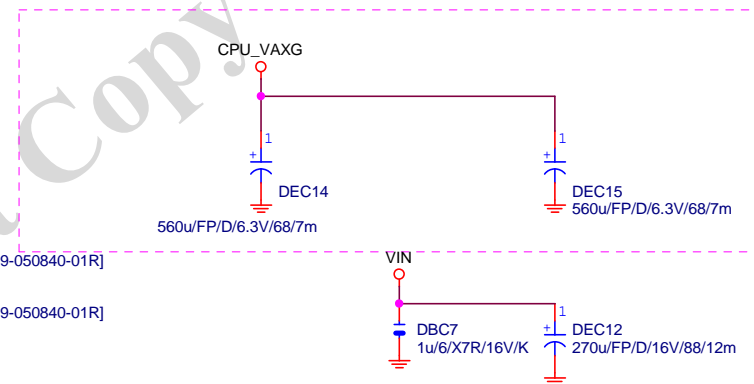
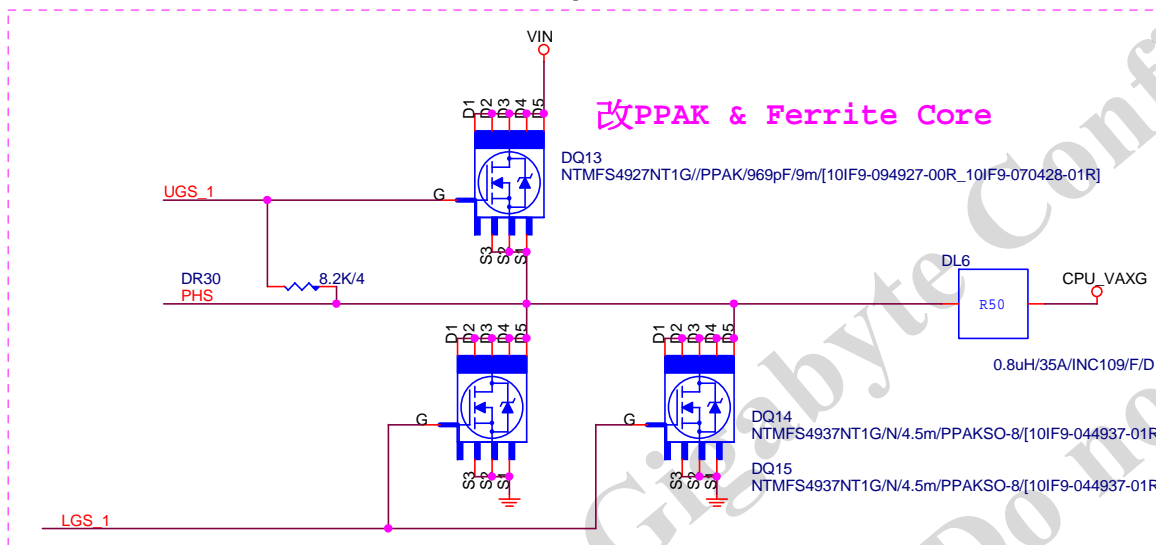
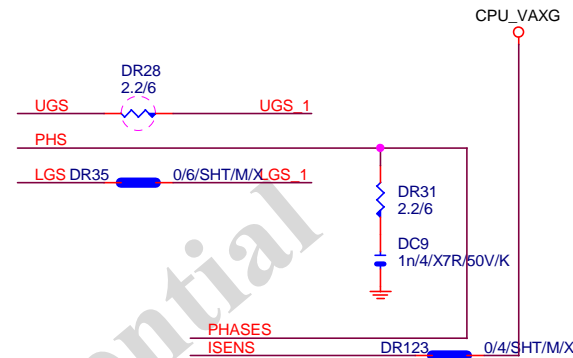
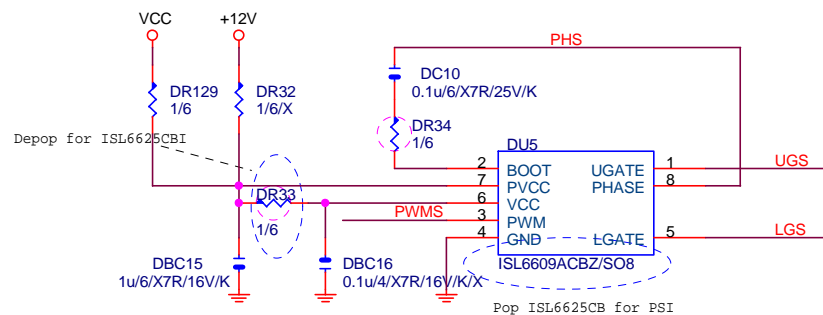
DR52 16.2K change to 24.9K

remove VAXG RDY



VAXG

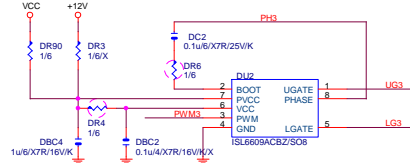
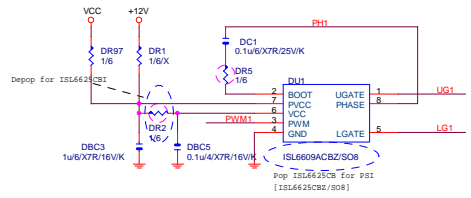
DR33 0 change to 1
DR34 0 change to 1
DR28 0 change to 2.2



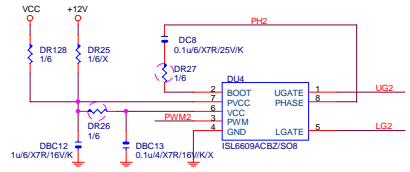
Gigabyte Technology

Title			
CPU CORE VR-2			
Size	Document Number	GA-H61M-D2H-USB3	
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DR5 0 change to 1
 DR2 0 change to 1
 DR4 0 change to 1
 DR6 0 change to 1



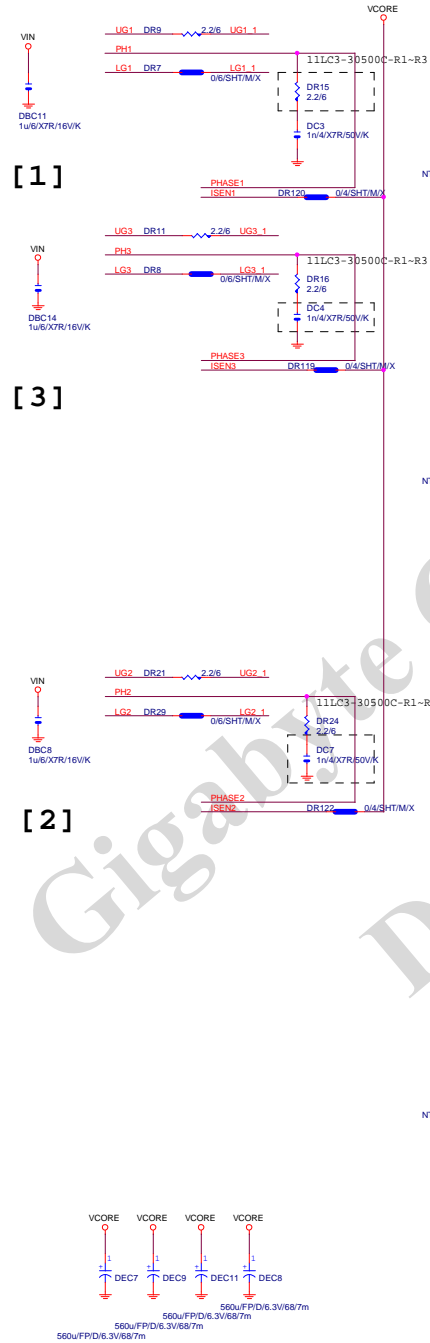
DR20 0 change to 1
 DR19 0 change to 1
 DR26 0 change to 1
 DR27 0 change to 1



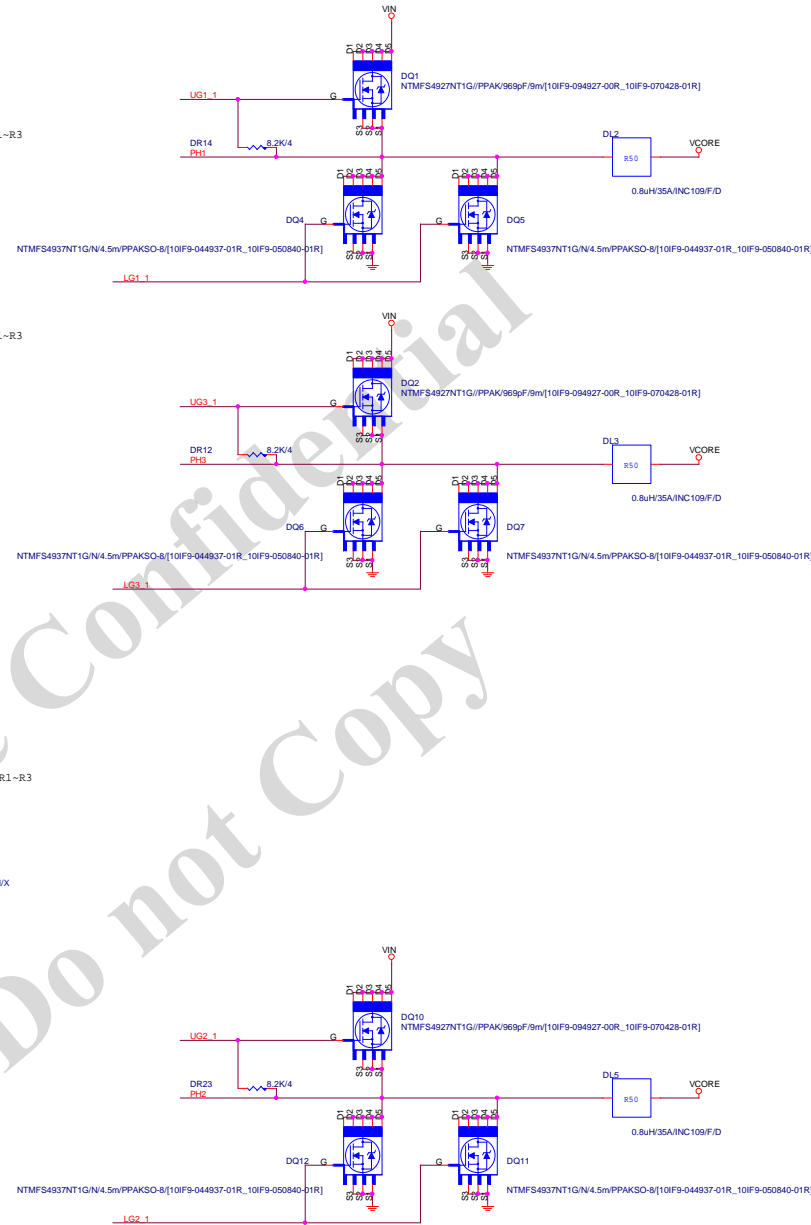
[1]

[3]

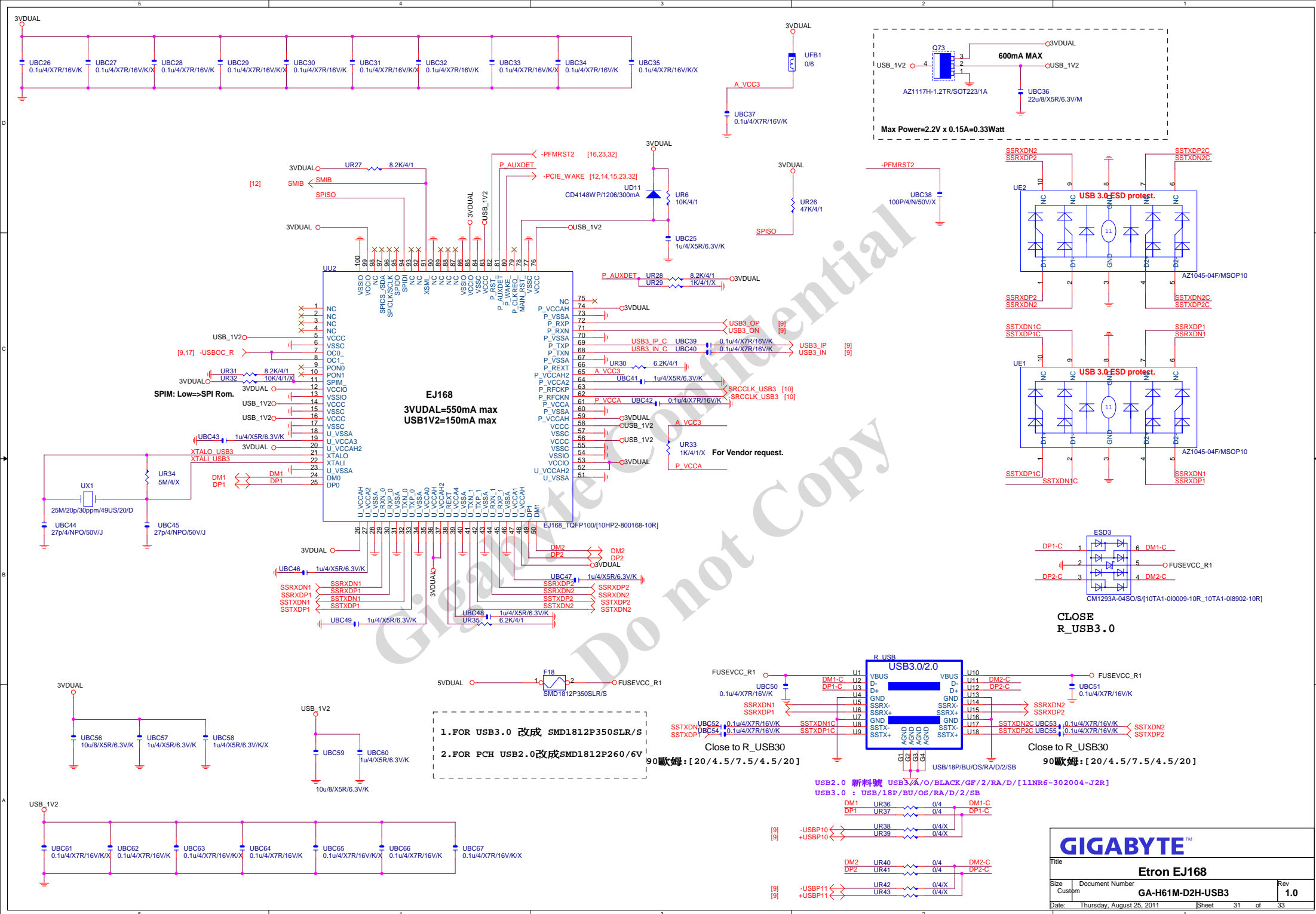
[2]



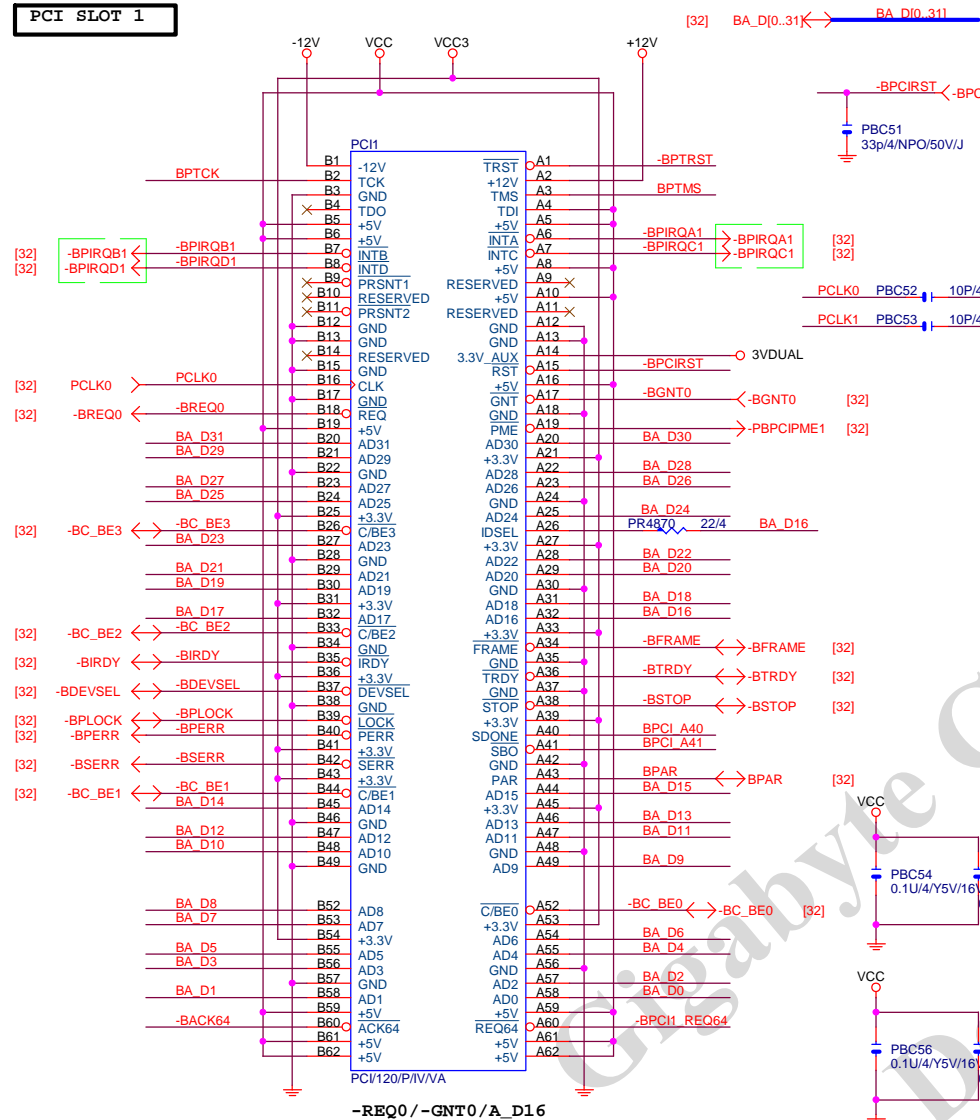
改PPAK & Ferrite Core



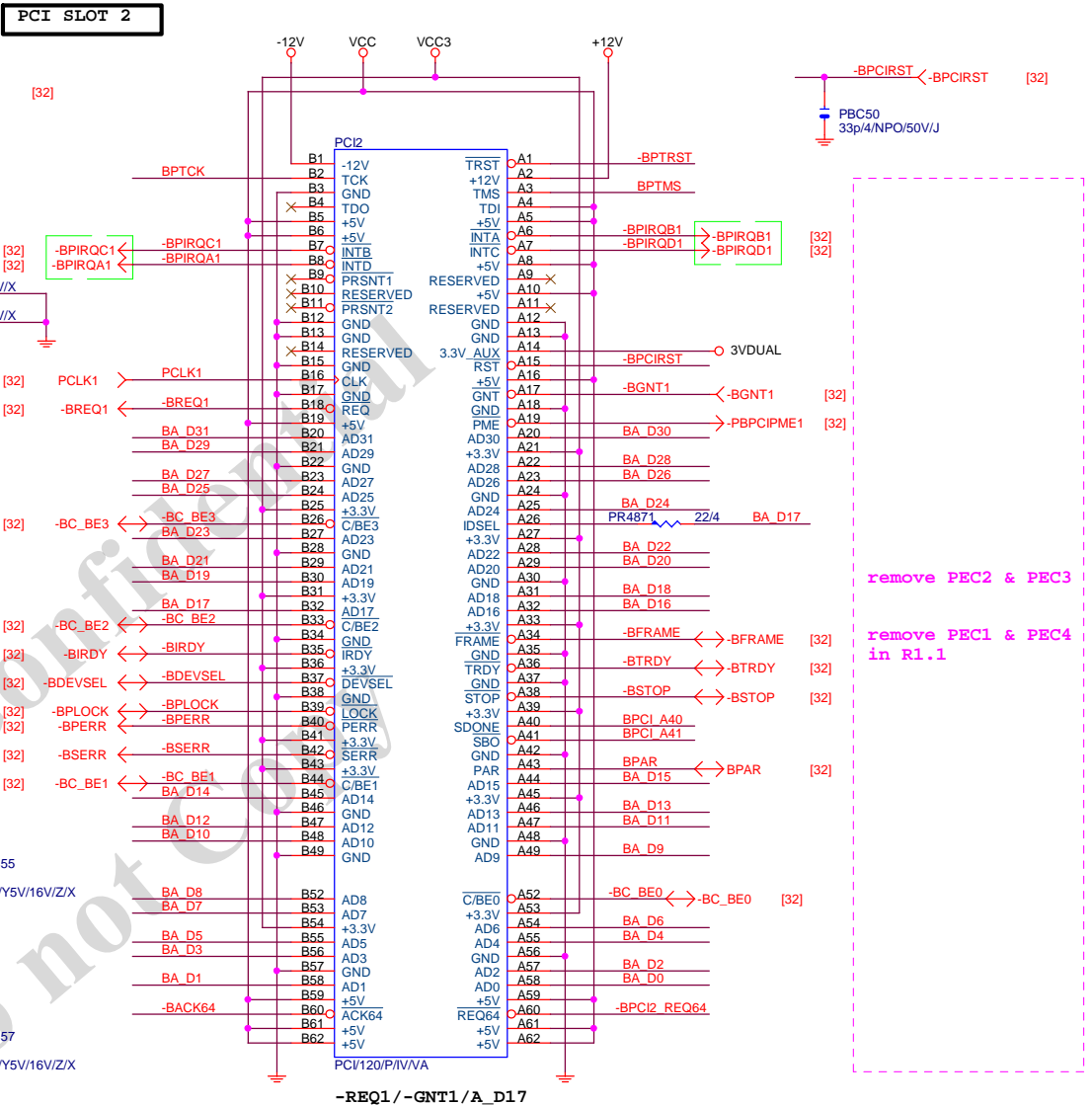
Gigabyte Technology			
CPU CORE VR-3			
Title	CPU CORE VR-3		
Size	Document Number	GA-H61M-D2H-USB3	Rev 1.0
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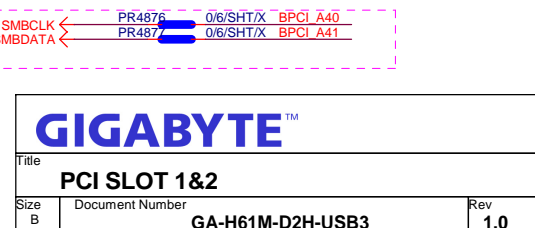
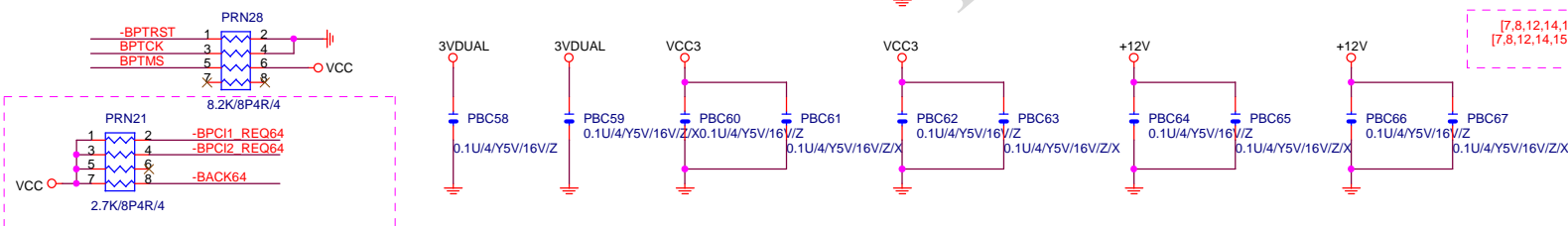
PCI SLOT 1



PCI SLOT 2



remove PEC2 & PEC3
remove PEC1 & PEC4
in R1.1



GIGABYTE™			
PCI SLOT 1&2			
Title	Document Number	Rev	
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